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APPLICATION NOTE

Upgrade Considerations from the 28F008SA to the 28F016SA

SALIM FEDEL
FLASH MEMORY APPLICATIONS ENGINEERING

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CONTENTS

PAGE

CONTENTS

PAGE

1.0 PURPOSE

The 28F016SA is the second member of Intel's FlashFile™ memory family. Its architecture evolved from that of the 28F008SA, Intel's first generation FlashFile memory device. The 28F016SA retains the standard 28F008SA's versatile capabilities and adds a Command Superset architecture which insures compatibility with the basic command-set.

This application note shows how to upgrade an existing 28F008SA-based design to the new 28F016SA memory device. Upgrades may require software modifications depending on the desired system functionality and straightforward hardware modifications to accommodate the new pinout.

2.0 SIMILARITIES AND DIFFERENCES BETWEEN THE 28F016SA AND THE 28F008SA

The 28F016SA memory is 100% command and algorithm, backward-compatible with the 28F008SA. It is defined as a Superset device which brings additional capabilities to system designs. Additional pins on the 28F016SA are added to define a user-selectable 8- or 16-bit wide memory, add on-chip write protection and multiple chip select signals. Note that you do not have to use the advanced features if you are performing a simple upgrade to the 28F016SA.

Before starting on your design upgrade, obtain the following specifications and application notes from Intel Corporation Literature Sales, 1 (800) 548-4725.

	Order #
28F008SA Data Sheet	290429
28F016SA Data Sheet	290489
28F016SA User's Manual	297372
28F008SA Software Drivers	292095
28F016SA Software Drivers	292126

2.1 Pinout Differences

Whereas the 28F008SA is 8-bit wide (40Ld-TSOP package), the 28F016SA is a high performance 16-bit wide flash file memory offering a user-configurable bus width (56Ld-TSOP package). Hence an additional 8 I/O pins are on the 28F016SA. Furthermore, the implementation of additional features such as Write Protect and Block Locking and user-selectable 3.3V and 5V operation require the definition of control pins for these functions. Finally, the optimization of the 28F016SA's architecture to achieve very high write performance resulted in a different pinout configuration from the 28F008SA.

Both device pinouts preserve the locations of I/O pins on the right-hand side and the sequence of pin functions of the 56Ld-TSOP package. However, it is still required to relay out an existing PCB design in order to accommodate the 16-Mbit chips. Table 1 lists all pin names and their numbers, highlighting all the changes.

Table 1. 28F008SA, 28F016SA Pin Comparison Chart

28F008SA Pin Name	28F016SA Pin Name	28F008SA 40L-TSOP	28F016SA 56L-TSOP	Notes
A_0	A_0	24	32	
A_1	A_1	23	28	
A_2	A_2	22	27	
A_3	A_3	21	26	
A_4	A_4	20	25	
A_5	A_5	19	24	
A_6	A_6	18	23	
A_7	A_7	17	22	
A_8	A_8	16	20	
A_9	A_9	15	19	
A_{10}	A_{10}	14	18	
A_{11}	A_{11}	13	17	
A_{12}	A_{12}	8	13	
A_{13}	A_{13}	7	12	
A_{14}	A_{14}	6	11	
A_{15}	A_{15}	5	10	
A_{16}	A_{16}	4	8	
A_{17}	A_{17}	3	7	
A_{18}	A_{18}	2	6	
A_{19}	A_{19}	1	5	
—	A_{20}	—	4	(Note 1)
DQ_0	DQ_0	25	33	
DQ_1	DQ_1	26	35	
DQ_2	DQ_2	27	38	
DQ_3	DQ_3	28	40	
DQ_4	DQ_4	32	44	
DQ_5	DQ_5	33	46	
DQ_6	DQ_6	34	49	
DQ_7	DQ_7	35	51	
—	DQ_8	—	34	
—	DQ_9	—	36	
—	DQ_{10}	—	39	
—	DQ_{11}	—	41	
—	DQ_{12}	—	45	
—	DQ_{13}	—	47	
—	DQ_{14}	—	50	
—	DQ_{15}	—	52	
CE#	CE_0#	9	14	
—	CE_1#	—	2	(Note 2)
RP#	RP#	12	16	(Note 3)
RY/BY#	RY/BY#	36	53	(Note 4)
OE#	OE#	37	54	
WE#	WE#	38	55	
—	BYTE#	—	31	(Note 5)
—	WP#	—	56	
—	3/5#	—	1	(Note 6)
V_{PP}	V_{PP}	11	15	
V_{SS}	V_{SS}	29, 30	21, 42, 48	
V_{CC}	V_{CC}	10, 31	9, 37, 43	
NC	NC	39, 40	3, 29, 30	

NOTES:
1. Highest Order Address
2. Dual CEx#
3. Formerly Called PWD#
4. Open Drain for 28F016SA
5. x8/x16 Selection
6. Selects Supply Voltage

CONFIGURATION

The following is an example which shows the state of all pins when operating in a 28F008SA-compatible mode:

WP# = V_{CC} (Write Protect feature disabled)
CE_0# = CE_1# (Chip Enable)
A_{20} = GND or V_{CC} (selects upper/lower 1 MB)
V_{CC} = 5.0V or 3.3V
BYTE# = GND (8-bit mode)
RY/BY# = Level Mode (set for default) with an external pull-up resistor

ation)

NOTE:
The 28F008SA has a CMOS driven RY/BY# output for interrupt capability.

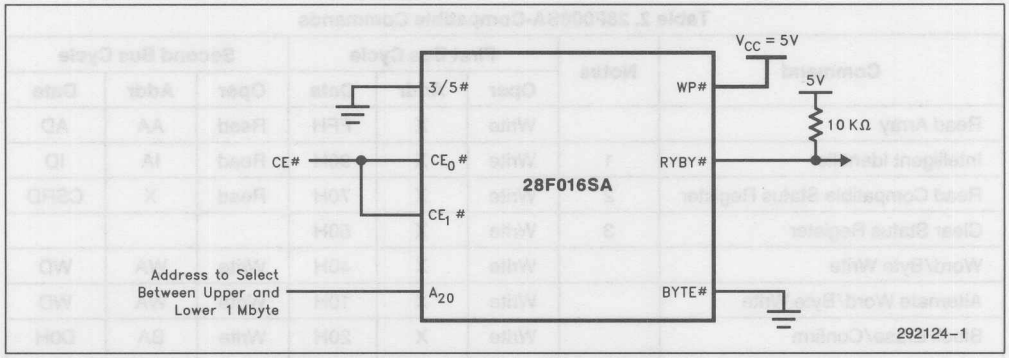


Figure 1. 28F016SA Configured as a 28F008SA-Compatible Memory

2.2 Compatible Command-Set

Byte Write	40H, 10H
Single Block Erase	20H
Erase Suspend to Read	B0H
Read Array	FFH
Read CSR	70H
Clear CSR	50H
Read Intelligent IDs	90H

Table 2. 28F008SA-Compatible Commands

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH	Read	AA	AD
Intelligent Identifier	1	Write	X	90H	Read	IA	ID
Read Compatible Status Register	2	Write	X	70H	Read	X	CSRD
Clear Status Register	3	Write	X	50H			
Word/Byte Write		Write	X	40H	Write	WA	WD
Alternate Word/Byte Write		Write	X	10H	Write	WA	WD
Block Erase/Confirm		Write	X	20H	Write	BA	D0H
Erase Suspend/Resume		Write	X	B0H	Write	X	D0H

ADDRESS
AA = Array Address
BA = Block Address
IA = Identifier Address
WA = Write Address
X = Don't Care

DATA
AD = Array Data
CSR = Compatible Status Register
CSRD = CSR Data
GSR = Global Status Register
BSR = Block Status Register
ID = Identifier Data
WD = Write Data

NOTES:
1. Following the Intelligent Identifier command, two Read operations access the manufacturer and device signature codes.
2. The CSR is automatically available after device enters Data Write, Erase, or Suspend operations.
3. Clears CSR.3, CSR.4 and CSR.5. Also clears GSR.5 and all BSR.5 and BSR.2 bits. See Status register definitions in the 28F016SA data sheet.

2.3 Technology Comparison

Both the 28F016SA and the 28F008SA are manufactured on Intel's Flash ETOX™ process technology. This technology is optimized for random access flash memory products with the highest read/write performance and lowest power consumption. The ETOX flash technology achieves very high reliability and quality.

2.4 Available Speeds

The 28F016SA designed on a 0.6 μm ETOX IV process, achieves faster speeds than the 28F008SA manufactured on 0.8 μm ETOX III process. Intel offers the 28F008SA in 5V-read version with speeds at 85/90 ns and 120 ns. The 28F016SA on the other hand is offered with a dual 3.3V and 5V read capability with speeds of (70/80 ns, 100 ns) and (120 ns, 150 ns) at 5V and 3.3V respectively. Note that both devices are offered at faster speeds (85 ns and 70 ns) under reduced loading conditions. *Please consult the data sheets referenced in this application note.*

2.5 Available Packages

The 28F016SA comes only in a 56Ld-Thin Small Outline Package (TSOP) optimized for its user-selectable x8/x16 memory architecture. The 28F008SA is offered in 2 packages, which are the 40Ld-TSOP (both standard and reverse pinout) and the 44Ld-Plastic Small Outline Package (PSOP).

2.6 Operating Modes

The 28F016SA behaves in the same manner as the 28F008SA. If a compatible command is written to the device, the Compatible Status Register contents are automatically put on the data bus. With the block locking disabled (WP# = high), the 28F016SA is identical to the 28F008SA, regardless of any lock-bit settings which define the lock state of a given block. The Command User Interface (CUI), Write State Machine (WSM) and Compatible Status Register (CSR) units function similarly on both devices.

The 28F016SA however, allows the user to issue multiple commands successively by watching the Queue bit (GSR.3 or BSR.3), a feature which improves performance, as described in the 28F016SA user's manual. Consult the 28F016SA data sheet and 28F016SA user's manual for detail operation.

2.7 AC Compatibility

The 28F016SA specifies the output Load circuit as an equivalent transmission line model which reflects the timing delays more accurately. The same diode/resistor circuit combination found in the 28F008SA data sheet also applies to the 28F016SA.

Address and Data are latched on the rising edge of WE# for both devices. All AC timing specifications are similar except for the differences noted in the data sheets. The 28F016SA has additional write timings describing the on-chip page buffers which do not exist on the 28F008SA.

2.8 DC Compatibility

Whereas the 28F008SA only operates at 5V V_{CC} and the 28F008SA-L only operates at 3.3V V_{CC}, the 28F016SA operates at both 3.3V and 5V V_{CC} supply voltages. In 5V mode of operation, the two devices are similar in terms of input/output level specifications. Consult the data sheets for differences in current consumption.

2.9 Power Considerations

In addition to the active, standby and deep power-down modes which exist on the 28F008SA, the 28F016SA has additional current modes useful in power management applications.

The two modes are:

Automatic Power Saving feature which is activated whenever the device addresses are not switching which is equivalent to a static mode of operation on the chip is accessed by a slowed clock. In this state, the chip typically draws less than 1 mA of total current.

The second low current mode of operation is enabled through command control, using the Sleep command. A Sleep command written to the device will put the chip in the lowest current state (deep power-down level) after all active operations have been processed. The device retains the value of its status registers while in sleep mode.

Note that the AC and DC specifications mentioned here are valid at the time this application note was written. Please reference the device data sheets for the latest up-to-date specifications.

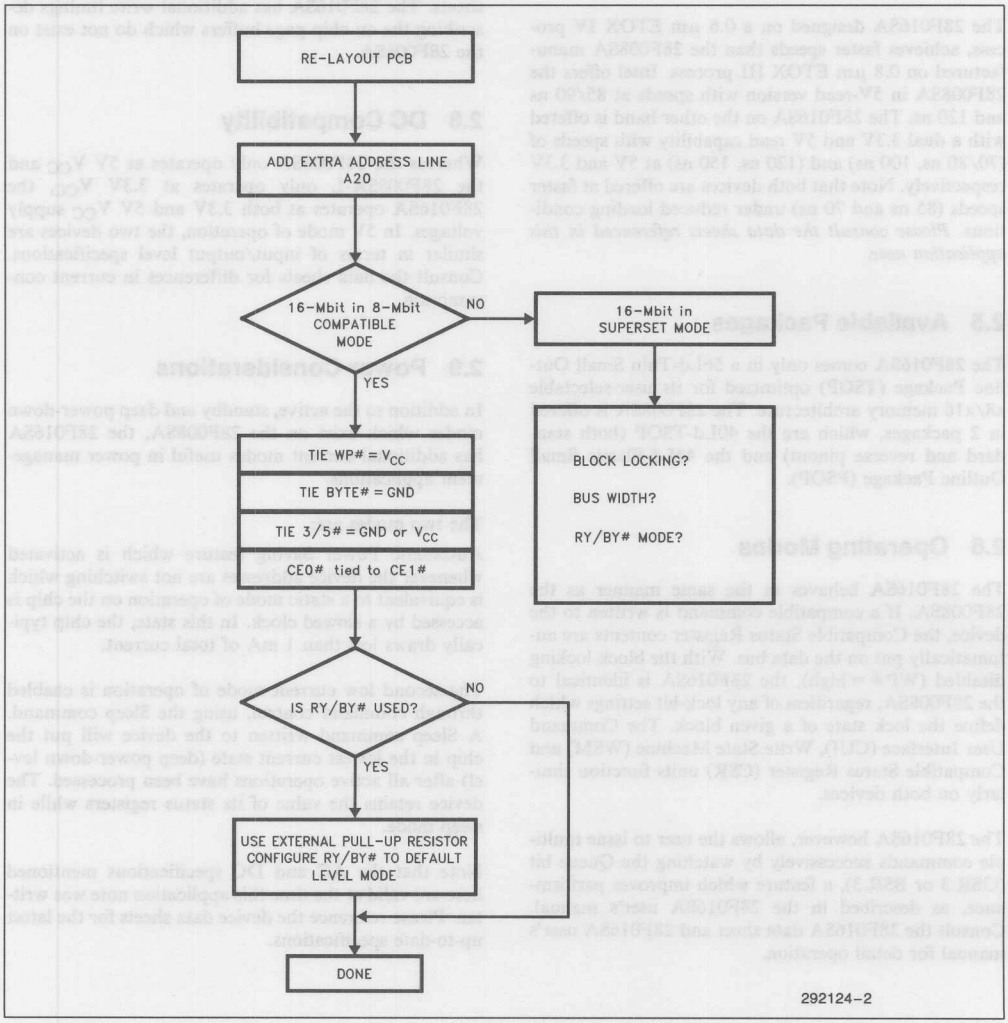
3.0 HARDWARE DESIGN CONSIDERATIONS

If you are considering a density upgrade to the 28F016SA, careful attention to certain areas must be followed. This section is not intended to cover all potential issues related to system design, but rather as a guideline in designing an upgrade to the 28F016SA.

3.1 Hardware Upgradability

The following flowchart summarizes the logical steps a system designer must go through to complete a density upgrade. This simple upgradability procedure allows the 28F016SA-based system to achieve quicker time-to-market while incorporating future expandability to take advantage of the Superset features of the 28F016SA.

3.2 Hardware Decision Flowchart



4.0 SOFTWARE DESIGN AND UPGRADABILITY CONSIDERATIONS

In order to do a software upgrade to the 28F016SA, the software designer must pay attention to a few key areas. They can be grouped as follows:

Device Intelligent Identifier = A0H (versus A2H for 28F008SA)

Compatible Superset Commands

Compatible Status Register Checks only

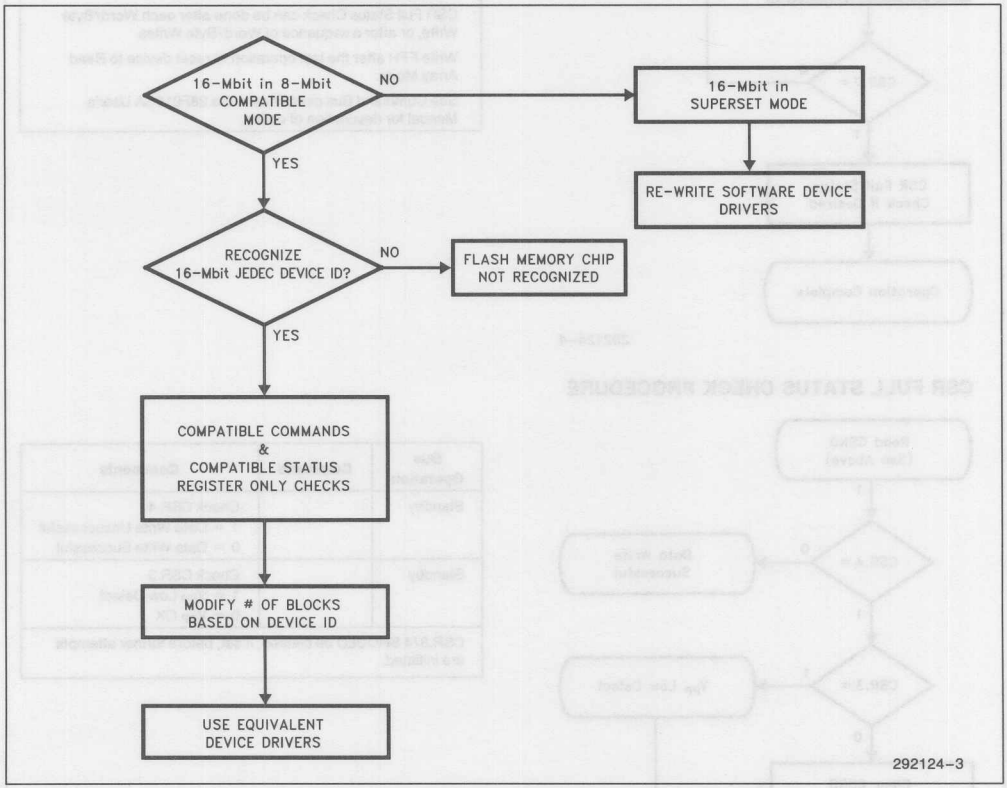
Number of Erase Blocks

Device Drivers for the 28F008SA and the 28F016SA are provided in application notes AP-360 and AP-377 respectively.

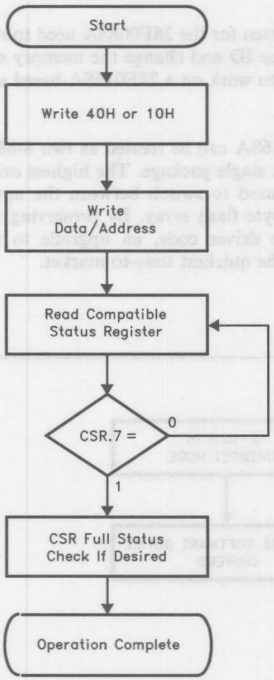
Software drivers written for the 28F008SA need to recognize the new device ID and change the memory size boundaries in order to work on a 28F016SA-based system design.

Note that the 28F016SA can be treated as two 8-Mbit memory devices in a single package. The highest order address pin A_{20} is used to switch between the upper and the lower 1 Mbyte flash array. By preserving the same basic software driver code, an upgrade to the 28F016SA enables the quickest time-to-market.

4.1 Software Decision Flowchart



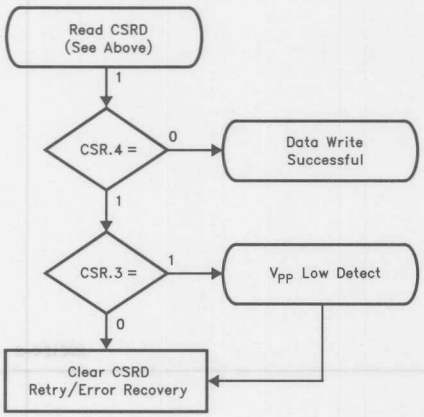
5.0 COMPATIBLE SOFTWARE ALGORITHM FLOWCHARTS



292124-4

Bus Operation	Command	Comments
Write	Word/Byte Write	D = 40H or 10H A = X
Write		D = WD A = WA
Read		Q = CSRD Toggle CE_0#, CE_1#, or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent Word/Byte Writes. CSR Full Status Check can be done after each Word/Byte Write, or after a sequence of Word/Byte Writes. Write FFH after the last operation to reset device to Read Array Mode. See Command Bus definitions in the 28F016SA User's Manual for description of codes.		

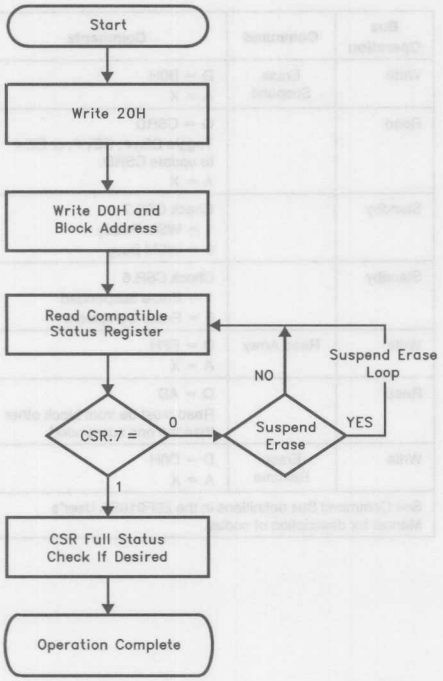
CSR FULL STATUS CHECK PROCEDURE



292124-5

Bus Operation	Command	Comments
Standby		Check CSR.4 1 = Data Write Unsuccessful 0 = Data Write Successful
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK
CSR.3/4 SHOULD be cleared, if set, before further attempts are initiated.		

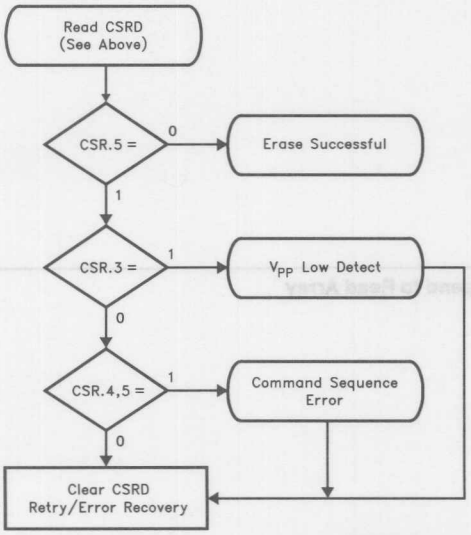
Figure 2. Word/Byte Writes



292124-6

Bus Operation	Command	Comments
Write	Block Erase	D = 20H A = X
Write	Confirm	D = D0H A = BA
Read		Q = CSRD Toggle CE_0#, CE_1#, or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent Block Erasures. CSR Full Status Check can be done after each Block Erase, or after a sequence of Block Erasures. Write FFH after the last operation to reset device to Read Array Mode. See Command Bus definitions in the 28F016SA User's Manual for description of codes.		

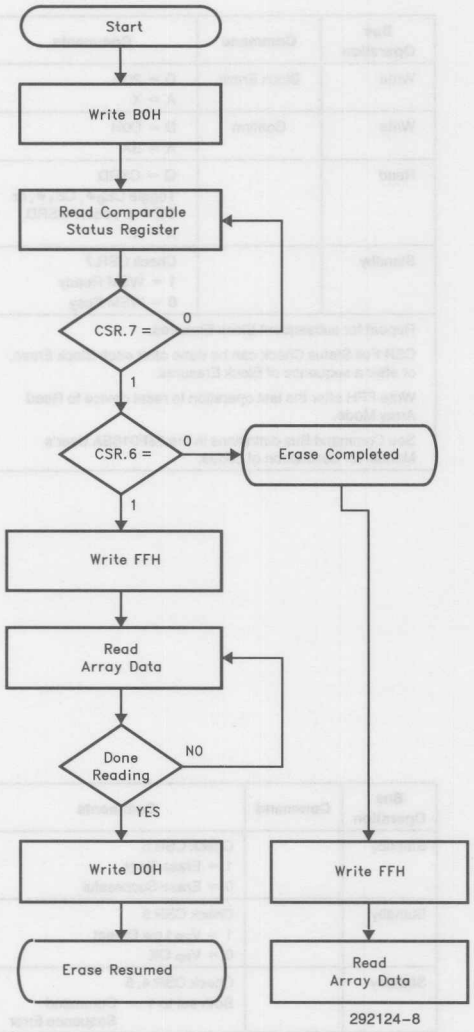
CSR FULL STATUS CHECK PROCEDURE



292124-7

Bus Operation	Command	Comments
Standby		Check CSR.5 1 = Erase Error 0 = Erase Successful
Standby		Check CSR.3 1 = V_{PP} Low Detect 0 = V_{PP} OK
Standby		Check CSR.4, 5 Both set to 1 = Command Sequence Error
CSR.3/4/5 SHOULD be cleared, if set, before further attempts are initiated.		

Figure 3. Block Erase



Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X
Read		Q = CSRD Toggle CE_0#, CE_1#, or OE# to update CSRD. A = X
Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A = X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X
See Command Bus definitions in the 28F016SA User's Manual for description of codes.		

Figure 4. Erase Suspend to Read Array

6.0 SUMMARY

This application note summarizes the upgrade considerations and compatibility areas between the 28F016SA and the 28F008SA. It is merely intended as a simple guideline to achieve a density and/or performance upgrade and to point out the key issues that the hardware and software designers must analyze during this process.

Consult the referenced documentation for a complete understanding of compatibility and device capabilities.

7.0 REFERENCES

Document	Order Number
28F016SA Data Sheet	290489
28F016SA User's Manual	297372
DD28F032SA Data Sheet	290490
AP-377 The 28F016SA Software Drivers	292126
AP-378 System Optimization using the Enhanced Features of the 28F016SA*	292127
AP-362 Implementing Mobile PC Designs Using High Density FlashFile™ Components	292097
ER-33 ETOX™IV Flash Memory Technology	294016
28F008SA 8 MB (1 MB x 8) FlashFile™ Memory Data Sheet	290429
AP-360 28F008SA FlashFile™ Software Drivers	292095
ER-27 The Intel 28F008SA FlashFile™ Memory	294011

NOTE:
*Check with Intel Literature Department for availability date

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